

CLAIMS:

1. Phase-switching dual modulus prescaler, comprising
a dual modulus divider (10) comprising:
 - a first and second divide-by-2 circuit (A;B), wherein said second divide-by-2 circuit (B) is coupled to the output of said first divide-by-2 circuit (A) and at least said
 - 5 second divide-by-two circuit (B) comprises four phase outputs (I_p , I_n , Q_p , Q_n ; IN_i , IN_{ni} , IN_q , IN_{nq}) each separated by 90° ;
 - a phase selection unit (PSU) for selecting one of the four phase outputs (I_p , I_n , Q_p , Q_n ; IN_i , IN_{ni} , IN_q , IN_{nq}) of the second divide-by-2 circuit (B);
 - a phase control unit (RTU) for providing control signal ($C1$, $NC0$; $C2$, $NC2$;
 - 10 $C3$, $NC3$) to the phase selection unit (PSU), wherein the phase selection unit (PSU) performs the selection of the four phase outputs (I_p , I_n , Q_p , Q_n ; IN_i , IN_{ni} , IN_q , IN_{nq}) according to the control signals ($C0$, $NC0$; $C1$, $NC1$; $C2$, $NC2$); and
 - said phase selection unit (PSU) is implemented based on direct logic.
- 15 2. Prescaler according to claim 1, wherein
 - the output (OUT) of the phase selection unit (PSU) is implemented according to the following logic code:
$$OUT = \overline{NC0} \bullet \overline{NC1} \bullet \overline{IN_i} + \overline{NC0} \bullet C1 \bullet \overline{IN_{ni}} + \overline{C0} \bullet NC2 \bullet \overline{IN_{nq}} + \overline{C0} \bullet C2 \bullet \overline{IN_q},$$
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- $+$, \bullet , $\overline{}$ represent an OR-, AND, and NAND functions, respectively.
- 3. Prescaler according to claim 1 or 2, further comprising
 - a divide-by-4 circuit (UA) coupled to the output of the phase selection unit
 - 25 (PSU), said divide-by-4 circuit (UA) comprises a sixth and seventh divide-by-2 circuit (F, G) each with four phase outputs (I_p , I_n , Q_p , Q_n) separated by 90° , said seventh divide-by-2 circuit (G) being coupled to the quadrature output (Q_p , Q_n) of the sixth divide-by-2.
- 4. Prescaler according to claim 1, 2 or 3, wherein

- the phase control unit (RTU) comprises a fourth and fifth divide-by-2 circuit (D, E) each with four phase outputs (I_p , I_n , Q_p , Q_n) separated by 90° , said fourth and fifth divide-by-2 circuit (D, E) being coupled in series,
 - the In-phase output signal (I_p , I_n) of the fifth divide-by-2 circuit (E)
5 corresponds to the control signal (C0),
 - the In-phase output signal (I_p , I_n) of the fourth divide-by-2 circuit (D) corresponds to the control signal (C1),
 - the quadrature phase output signal (Q_p , Q_n) of the fourth divide-by-2 circuit (E) corresponds to the control signal (C2).
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5. Prescaler according to claim 4, wherein
- the phase control unit (RTU) further comprises a D-latch (DL) coupled to the input of the fifth divide-by-2 circuit (E),
 - the D-latch (DL) receives the previous state of the In-phase output (I_p , I_n) of
15 the seventh divide-by-2 circuit (G) and a signal (modul) indicating the number of phase switching as input signals.
6. Prescaler according to claim 1, wherein said dual modulus divider (10) is a 16/17 divider.
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7. Prescaler according to claim 1, further comprising a synchronization loop coupled to the dual modulus divider (10) for reclocking the dual modulus divider (10).
8. Frequency synthesizer comprising a prescaler according to any one of the
25 claims 1 to 7.